



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

James D.Y. COLLIER et al.

Serial No.: 09/618,296

Filed: July 18, 2000

For: VARIABLE OSCILLATOR

Examiner: David Q. Nguyen

Group Art Unit: 2681

**DECLARATION UNDER 37 C.F.R. § 1.131**

We, James Digby Yarlet Collier and Ian Michael Sabberton, the inventors in the above-captioned patent application, hereby respectfully submit this declaration to overcome the Endo et al. prior art reference relied upon by the Examiner in the Office action of October 24, 2002 specifically, U.S. Patent No. 6,172,576 to Endo et al., having a filing date of April 2, 1999. To that end, we hereby declare as follows:

1. We incorporate herein by reference our prior declaration under 37 CFR § 1.131 filed in the subject application on 24 April 2003, which establishes conception of the claimed invention prior to April 2, 1999.

2. During the period of time the subject matter of this application was being developed, we were employed by Cambridge Silicon Radio, Ltd. (CSR) of Cambridge, England, the assignee of this application.

3. The subject matter of this application was developed in conjunction with the CSR single chip bluetooth device known as BlueCore 01b.

4. A laboratory notebook was kept by us in connection with the development of the subject matter of this application.

5. Copies of certain pages of that notebook, which were prepared between a date prior to April 2, 1999 and July 19, 1999, the filing date of UK Patent Application No. 9916907.0, which is claimed as priority under 35 U.S.C. § 119 ("the priority application"), are attached to this declaration at Exhibit A.

6. These pages demonstrate that we acted with due diligence toward the development of the subject matter of the claims of this application from a time prior to April 2, 1999 through July 19, 1999, the filing date of the priority application. In particular, the attached handwritten notes reflect that continuous design development work and experimental testing were performed between April 2, 1999 and July 19, 1999.

7. Moreover, the pages show various drawings illustrating various configuration options for a variable oscillator that were conceived and evaluated. These drawings correspond to the embodiments of the invention as shown in Figs. 1-5 of the present application.

**DECLARATION UNDER 37 C.F.R. § 1.68**

All statements made herein of our own knowledge are true and all statements made on information and belief are believed to be true. We understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of this application or any patent issuing thereon.

James Collier

James D. Y. Collier

14 February 2005

Date

I. Michael Sabberton

Ian Michael Sabberton

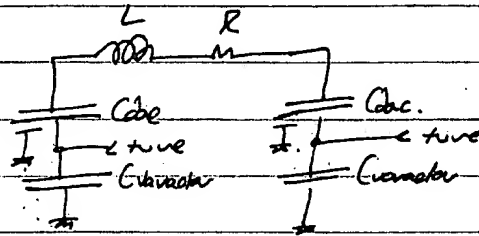
14 February 2005

Date

# VCO (phase) Trim structure.

18 March 99.

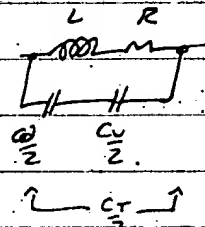
Circuit:-



Tolerances: require constant loop gain over process.

$$\Rightarrow \frac{d\omega}{dV_{tune}} = \text{constant.}$$

analyse model network as



$$C_T = \frac{C_u C_v}{C_u + C_v}$$

$$\omega^2 = \frac{2 \cdot L - R^2 C_T}{C_T L^2}$$

$$= \frac{2 \frac{L}{C_T} - R^2}{L^2}$$

$$\frac{d\omega}{dC_T} = \frac{1}{2} \left( \frac{2 \frac{L}{C_T} - R^2}{L^2} \right)^{-1/2} \left( \frac{-2}{L C_T^2} \right)$$

$$= \frac{-1}{C_T^2 \left( \frac{2 \frac{L}{C_T} - R^2} \right)^{1/2}} \Rightarrow \frac{d\omega}{dC_T} = \frac{-1}{C_T^2 \omega \cdot L}$$

$$\frac{d\omega}{dC_u} = \frac{d\omega}{dC_T} \frac{dC_T}{dC_u}$$

$$\frac{dC_T}{dC_u} = \frac{C_v^2}{(C_u + C_v)^2}$$

$$\therefore \frac{d\omega}{dC_u} = \frac{-C_v^2}{(C_u + C_v)^2} \cdot \frac{1}{\omega \cdot L} \cdot \frac{(C_u + C_v)^2}{C_u^2 C_v} = \frac{-1}{\omega \cdot L \cdot C_u^2}$$

$\Rightarrow$  for constant  $\frac{d\omega}{dC_u}$  at fixed  $\omega$  requires  $L \propto \frac{1}{C_u^2}$

PTO  
- L ->

# VO Triun Continued.

$$\text{have } \frac{dw}{dC_v} = \frac{-1}{w \cdot L \cdot C_v^2}$$

want constant  $\frac{dw}{dV_{th}}$ ,  $\Rightarrow$  require knowledge about  $\frac{dC_v}{dV_{th}}$  for varactor.

i.e. ideal (ish) case.  $C_v = C_{v0} \cdot \frac{1}{(1 - V_F/\phi)^n}$  zero bias capacitance  
 $\nwarrow$  assume  $n = 1/2$ .

$$\text{then } \frac{dC_v}{dV_F} = \frac{C_{v0}}{2\phi(1 - V_F/\phi)^{3/2}}$$

$\uparrow$   
 $(V_F = V_{th})$

$$\Rightarrow \frac{dw}{dV_{th}} = \frac{C_{v0}}{2\phi(1 - V_{th}/\phi)^{3/2}} \cdot \frac{1}{w \cdot L} \cdot \frac{((1 - V_F/\phi)^{1/2})^n}{C_{v0}^n}$$

$$= \frac{-1}{2C_{v0}\phi(1 - \frac{V_{th}}{\phi})^{1/2} \cdot w \cdot L}$$

if  $V_{th} = -1V$  at  $L = 0$ , assume  $\phi = 0.5V$ .

what is  $V_{th}$  at  $L = +108$  for same  $\frac{dw}{dV_{th}}$ ?

$$\frac{dw}{dV_{th}} \propto \frac{-1}{L \cdot (1 - \frac{V_{th}}{\phi})^{1/2}}$$

$\therefore$  if  $L = +108$   $V_{th} \approx 0.7V$ .

$\Rightarrow$   $\leftarrow$  smaller  $\rightarrow$  larger  $\Rightarrow C$  = smaller for same  $w$ .

ii, ST varactor model.  $\phi \approx 0.5V$   
 $n \approx 1/3$ .

$$\frac{\partial C_v}{\partial V_F} = \frac{C_{v0}}{3\phi \left(1 - \frac{V_F}{\phi}\right)^{4/3}}$$

$$\Rightarrow \frac{\partial \omega}{\partial V_{tue}} = \frac{f_{v0}}{3\phi \left(1 - \frac{V_F}{\phi}\right)^{4/3}} \cdot \frac{-1}{\omega \cdot L} \cdot \frac{\left(1 - \frac{V_F}{\phi}\right)^{2/3}}{C_{v0}}$$

$$\frac{\partial \omega}{\partial V_{tue}} = \frac{-1}{3C_{v0}\phi \left(1 - \frac{V_F}{\phi}\right)^{2/3} \cdot \omega \cdot L}$$

if  $V_{tue} = 1V$  at  $L$  norm, what is  $V_{tue}$  at  $L = +10\%$ .

$$\frac{\partial \omega}{\partial V_{tue}} \propto \frac{-1}{L \left(1 - \frac{V_{tue}}{\phi}\right)^{2/3}}$$

$\therefore$  if  $L = +10\%$   $V_{tue} = 0.69V$ .

$\Rightarrow$  Capacitor is at  $+10\%$ ,  $L$  at  $+10\%$   $\Rightarrow$  CD low.

$(-10\%, V_{tue} = 1.26V, \text{Capacitor at } -10\% \Rightarrow \text{CD high})$

- \* simulation to check constant dfreq/dVbias of varactor tuned pierce
- \* oscillator

```

* circuit :-
*
*
*      --- ind ---
*      |
*      C1
*
*      C2
*
*      xCv1
*
*      xCv2
*
*      Gnd
*
*
*      expect dfreq/dCv = -1 / (Cv^2*Pres* Lind)
*      freq and Pres (resonant freq) in rad/sec

```

```

* inductor Q of 10 at 1GHz
l1 tl nl IND
xl nl t2 6
.param IND=10n
* Capacitor networks 5pF eq each (2.5p eff load across ind)
cc1 tl ncl CDAC
xcv1 0 ncl 0 val48m1
cc2 t2 nc2 CDAC
xcv2 0 nc2 0 val48m1
.param CDAC=8p
*
vtune tune 0 BIAS
.param BIAS=0
rtune1 ncl tune 10a3
rtune2 nc2 tune 10e3
* dummies
rd3 tl 0 1e9

```

```
* drive
idrive t1 t2 0 ac 1
```

```

.ac    lin 5000 750e6 1.25e9
.step param BIAS 0.5 2.0 0.25

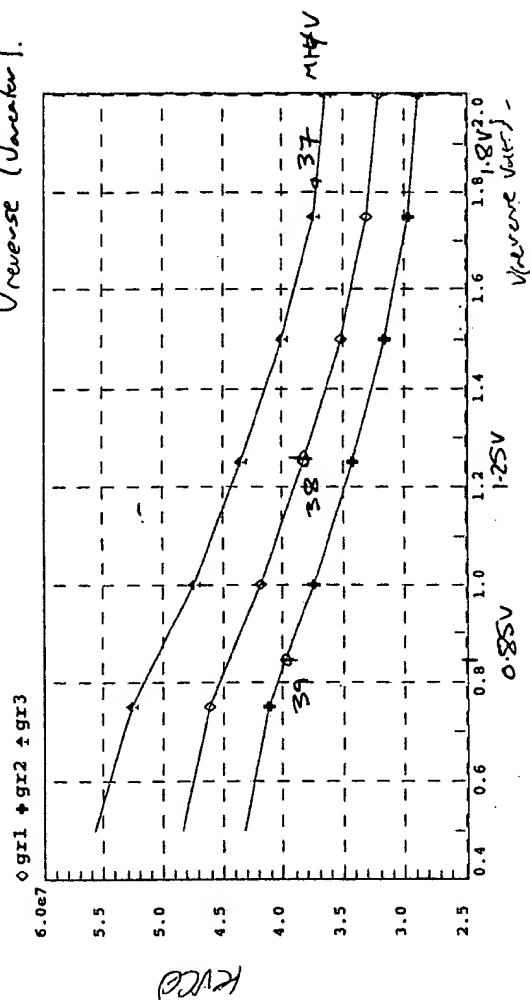
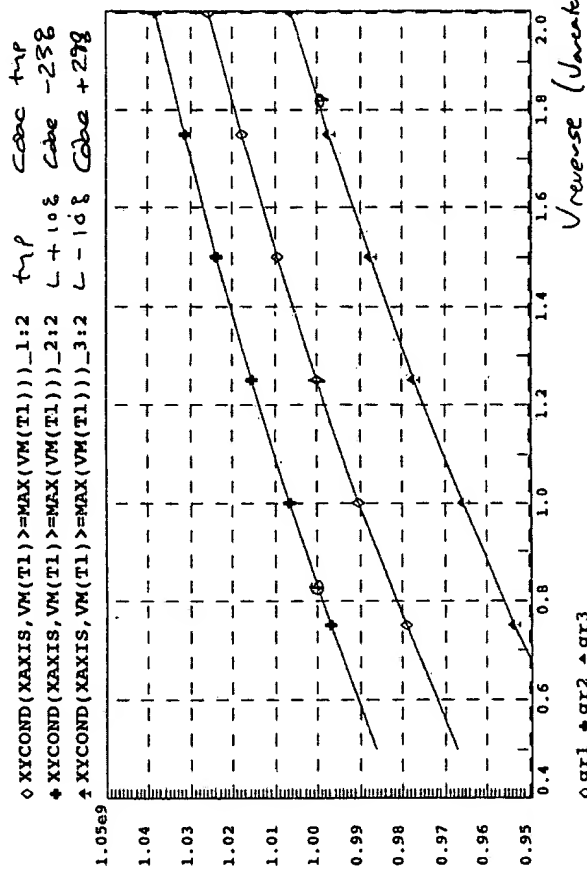
```

```
plot ac vdb(t1) vdb(t2)
extract xycond(xaxis, vm(t1) >= max(vm(t1)))
```

lib	/home/csrad/process/st/bicmos_0u35/eldo/capacitor.lib	varactor_type
lib	/home/csrad/process/st/bicmos_0u35/eldo/capacitor.lib	varactor_type

```
alter      INB-11n  
param     CDAC-6.6p  
param
```

```
alter
param IND=9n
param CDAC=10.3p
```



Constant VCB constant for VCB indicator over  $\pm 10\%$  range, achieved by adjusting variable sensitivity point and (fixed per unit).

Target frequency:  $1.2256 \text{ GHz} \pm 20 \text{ MHz}$  pull.

KVCO:  $10 \text{ MHz/V}$ .

want KVCO independent of channel:  $L \approx 5 \text{ nH}$ .

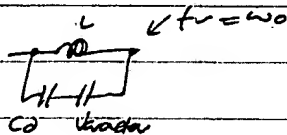
from previous page:  $\frac{d\omega}{dV_{tune}}$

$$= \frac{-1}{3C_0\phi \left(1 - \frac{V_t}{\phi}\right)^{3/2} \omega_0 L}$$

for varactor with

$m = 1/3$  (like ST part).

for



$\Rightarrow$  for  $10 \text{ MHz/V}$   $C_0 = 69 \text{ pF}$  @  $V_t = -1 \text{ V}$ .

$C_{varactor @ -1V} = 48 \text{ pF}$ .

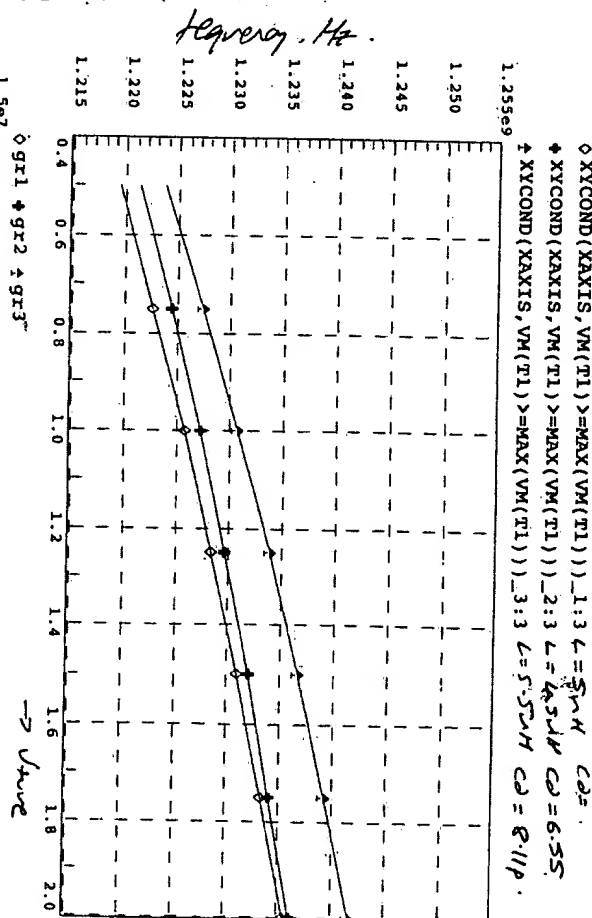
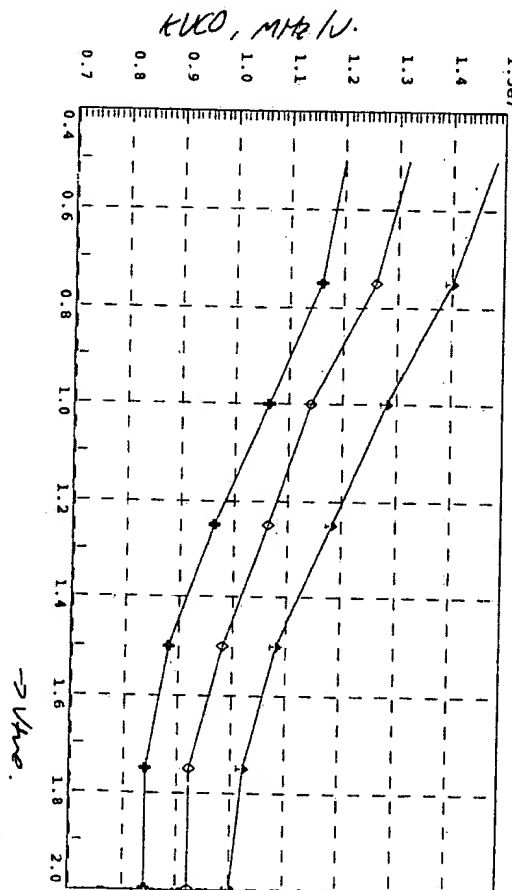
$\Rightarrow C_0 = 3.65 \text{ pF}$ .

change  $L$  to  $5.5 \text{ nH} \Rightarrow +10\%$  if Varactor at  $1 \text{ V}$  still  $\Rightarrow \frac{d\omega}{dV_{tune}}$  at  $9.0\%$ .

"  $4.5 \text{ nH} \Rightarrow -10\%$

"  $110\%$ .

continued below:



$\frac{d\omega}{dV_{tune}} = \frac{C_0}{C_0 + C_{varactor}}$

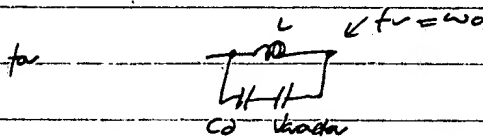


Target: frequency  $1.2256\text{GHz} \pm 20\text{MHz}$  pull.

KVCO  $10\text{MHz/V}$ .

want KVCO independent of channel:  $L \geq 5\text{nH}$ .

from previous page:  $\frac{d\omega}{dV_{\text{tune}}} = \frac{-1}{3C_0\phi(1-\frac{V_t}{\phi})^{3/2} \cdot \omega_0 L}$  for varactor with  $m=1/3$  (like ST part).



$\Rightarrow$  for  $10\text{MHz/V}$   $C_0 = 69\text{pF}$  @  $V_t = -1\text{V}$ .

$C_{\text{varactor}} @ -1\text{V} = 48\text{pF}$ .

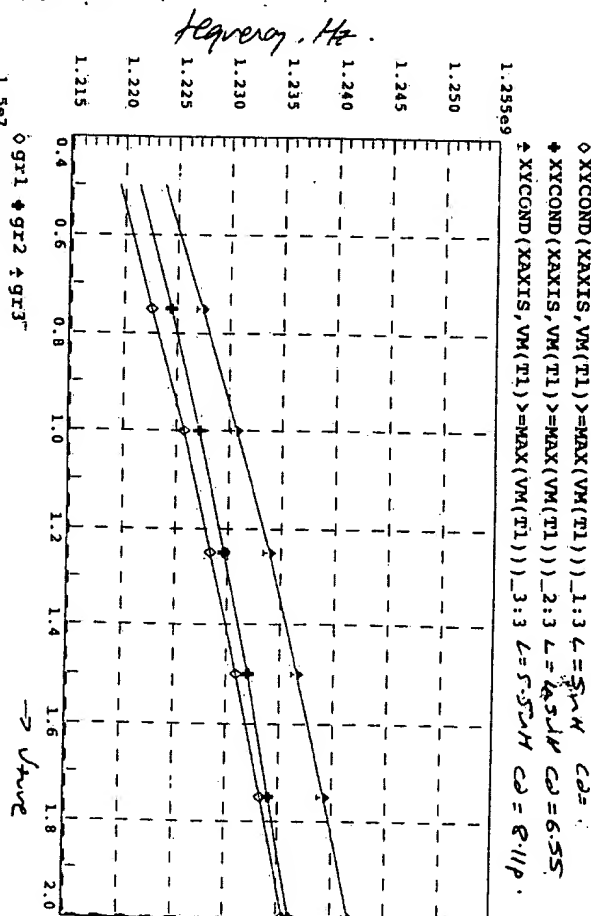
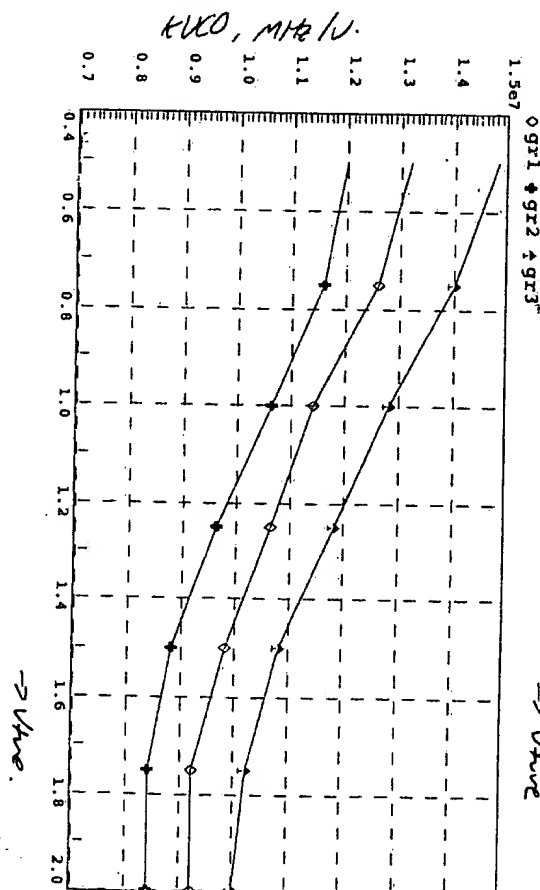
$\Rightarrow C_0 = 3.65\text{pF}$ .

change  $L$  to  $5.5\text{nH} \Rightarrow +10\%$  if Varactor at  $1\text{V}$  still  $\Rightarrow \frac{d\omega}{dV_{\text{tune}}}$  at  $9.0\%$ .

"  $4.5\text{nH} \Rightarrow -10\%$

"  $110\%$

continued below:

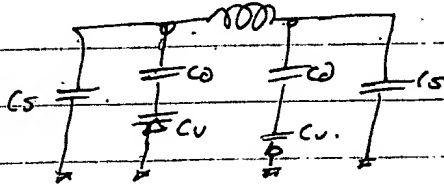


$\frac{d\omega}{dV_{\text{tune}}} = \frac{1}{C_0} \frac{dC_0}{dV_{\text{tune}}}$

0: XXCOND(XAXIS, VM(T1)) = MAX(VM(T1)) 1:3 L = 5.5nH C0 = 3.65pF  
 + XXCOND(XAXIS, VM(T1)) = MAX(VM(T1)) 2:3 L = 5nH C0 = 6.55pF  
 + XXCOND(XAXIS, VM(T1)) = MAX(VM(T1)) 3:3 L = 4.5nH C0 = 8.11pF

NO answer.

Previous showed good performance although the need for a large capacitor,  $2 \times 140 \text{ pF}$  in precise designation. Try :-



$$\left[ \frac{C_T}{C_S} \right] \rightarrow C_T = \frac{C_S(C_D + C_U) + C_D C_U}{C_D + C_U}$$

reflecting the fact that there are two of the above <sup>opposite</sup> network in series :-

$$\frac{dC_T}{dC_U} = \frac{C_D^2}{(C_D + C_U)^2}$$

$$\frac{dC_U}{dC_U} = \frac{C_D^2}{\omega \cdot L \cdot (C_S(C_D + C_U) + C_D C_U)^2}$$

assuming  $C_U \gg C_S, C_D$ .

$$\rightarrow \frac{C_D^2}{\omega \cdot L \cdot C_U^2 (C_S + C_D)^2}$$

from previous

$$C_U = \frac{C_{U0}}{(1 + V_{t/\phi})^{1/3}} \quad \& \quad \frac{dC_U}{dV_F} = \frac{C_{U0}}{3\phi(1 + V_{t/\phi})^{4/3}}$$

$$\therefore \frac{dC_U}{dV_F} = \frac{C_D^2}{\omega \cdot L \cdot C_{U0} (C_S + C_D)^2 3 \cdot \phi (1 + V_{t/\phi})^{2/3}}$$

= previous result scaled by  $\frac{C_D^2}{(C_S + C_D)^2}$

Want to reduce capacitor size by factor 3, but keep the same  $KV_{CO}$  at 1.225 GHz.

$$\Rightarrow \frac{C_D^2}{(C_S + C_D)^2} = \frac{1}{3}$$

$$\Rightarrow C_D = 1.37 \cdot C_S$$

$$L = 5n, C_T = 3.38pF \text{ (1.225 GHz)}, C_V = 16pF \text{ (or 1V V4)}.$$

$$\Rightarrow C_S = 1.53pF \Rightarrow C_D = 2.10pF.$$

$$\text{in piece want } \Rightarrow C_S = 3.1p, C_D = 4.2pF.$$

if  $L$  is at +10%,  $C_S$  at +10%. (process exchange) ( $C_V$  same).

What is value of  $C_D$  and  $KV_{CO}$ ?

$$\text{New } C_T = 3.07pF \text{ (for 1.225 GHz)}, C_S = 3.4pF, C_V = 16pF.$$

$$\Rightarrow C_D = 1.53pF \text{ (x2 = 3.07pF)}$$

$$\frac{\partial K}{\partial t} = x \cdot \frac{1}{1.1} \times \frac{0.224}{0.333} \times \frac{C_D^2}{(C_S + C_D)^2} \text{ vato.} = x \cdot \frac{0.61}{0.333} \text{ previous vato}$$

61% of  $KV_{CO}$

$$(S_{mi} \Rightarrow 0.62)$$

repeat  $L$  at -10%,  $C_S$  at -10%.

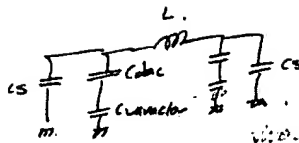
$$\text{New } C_T \text{ (for 1.225 GHz) is } 3.75pF, C_S = 1.4pF, C_V = 16pF.$$

$$\Rightarrow C_D = 2.75pF \text{ (x2 = 5.5pF)}$$

$$\frac{\partial K}{\partial t} = x \cdot \frac{1}{0.9} \times \frac{0.439}{0.333} = x \cdot 1.47$$

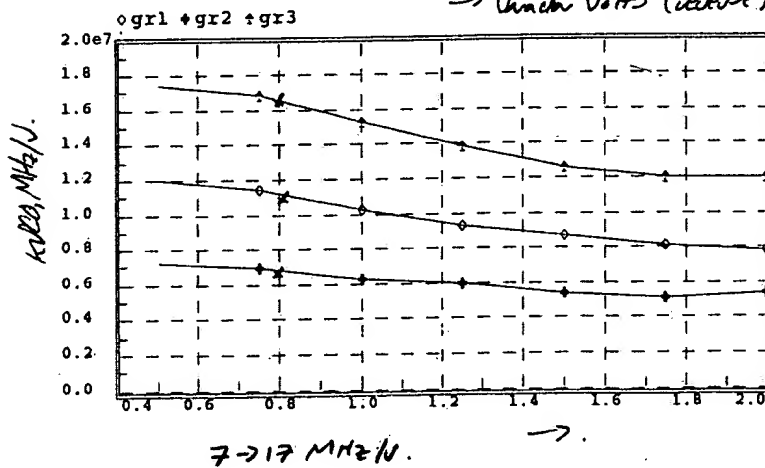
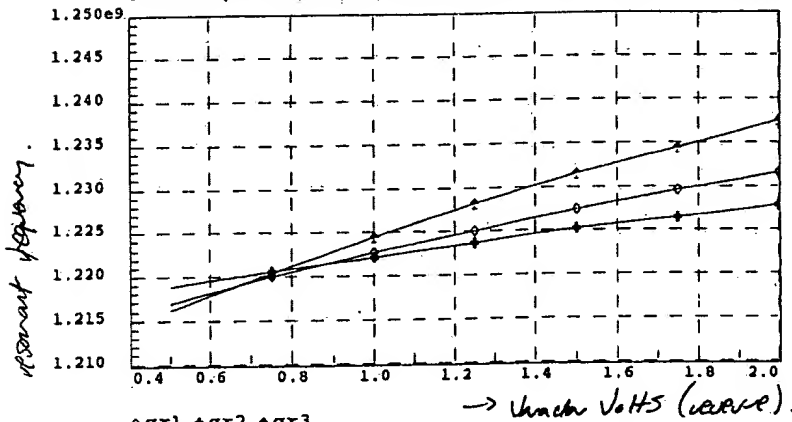
147% of  $KV_{CO}$ .

Results are:



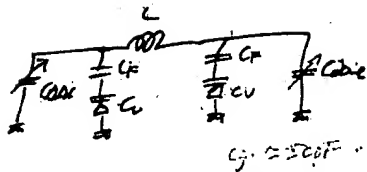
W.D. 50 = 2 x 10<sup>-6</sup> sec, L<sub>0</sub> = 2.5 nH

◊ XYCOND(XAXIS, VM(T1))>=MAX(VM(T1))\_1:9 5n, CS=3.1p C<sub>load</sub>=4.2p.  
 ♦ XYCOND(XAXIS, VM(T1))>=MAX(VM(T1))\_2:9 5.5n, CS=3.4p C<sub>load</sub>=3.05p.  
 † XYCOND(XAXIS, VM(T1))>=MAX(VM(T1))\_3:9 4.5n, CS=2.8p C<sub>load</sub>=5.6p.

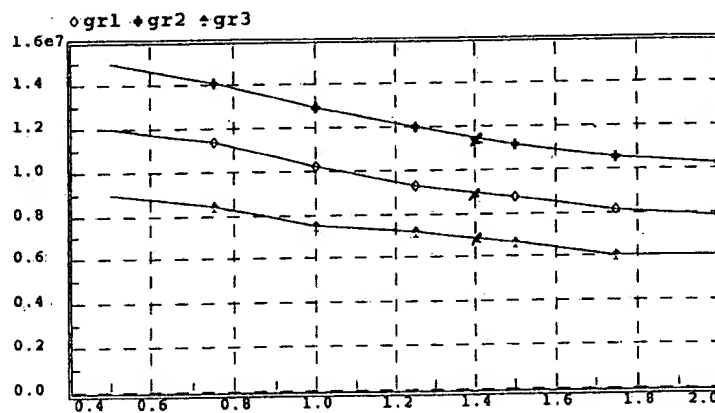
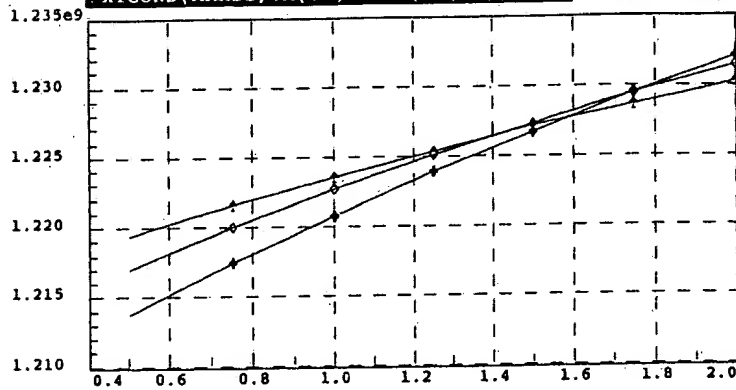


Simulation shows variation in KUCO for process tolerance of inductance and capacitance, (S. large by 10% for inductance large by 10% + diff for -10%.

KUCO variation too large.



$C_1 = 500 \text{ pF}$   
 $\diamond \text{XYCOND}(\text{XAXIS}, \text{VM}(\text{T1}) > \text{MAX}(\text{VM}(\text{T1})))\_1:1 \quad L=5\text{n} \quad C=4.2\text{p} \quad C_{\text{drc}}=3.1\text{p}$   
 $\diamond \text{XYCOND}(\text{XAXIS}, \text{VM}(\text{T1}) > \text{MAX}(\text{VM}(\text{T1})))\_2:1 \quad L=5.5\text{n} \quad C=4.8\text{p} \quad C_{\text{drc}}=2.2\text{p}$   
 $\diamond \text{XYCOND}(\text{XAXIS}, \text{VM}(\text{T1}) > \text{MAX}(\text{VM}(\text{T1})))\_3:1 \quad L=6.5\text{n} \quad C=3.8\text{p} \quad C_{\text{drc}}=4.15\text{p}$



$f \rightarrow 11.5 \text{ MHz/V}$

Report of previous except fixed capacitance in series with variable. Capacitors and inductance  
 tolerance swept together for worst case. Variation is 1000 much reduced.

Final VCO Tun tolerance.

22 March 94.

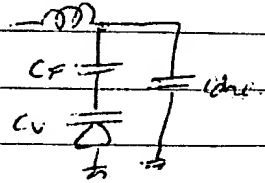
Want KVCO  $\approx 10 \text{ MHz/V}$  at  $1.225 \text{ MHz}$ . Single Variator per side

previous tolerance  $\Rightarrow 8.12 \text{ MHz/V}$  with process.

Capacitor  $\approx 16 \text{ pF}$  at  $1 \text{ V}$  reverse.

Fixed capacitor in with variator,  $C_{\text{dnc}}$  to ground.

Want Variator voltage within spec.



$0.6 \times 8.12 \text{ MHz/V} \Rightarrow C_{\text{dnc}}$  to tune to nearest  $4.8 \text{ MHz}$ .

from previous page for  $10 \text{ MHz/V}$ ,  $C_F = 3.3 \text{ pF} \approx C_{\text{dnc}}$ .

SWH requires  $3.38 \text{ pF}$  turn  $\Rightarrow 6.76 \text{ pF}$  (2 in ser).

$C_F = 3.3 \text{ pF}$ .

$\Rightarrow C_F \text{ ser } C_U = 2.7 \text{ pF}$ .

(nom).  $\Rightarrow C_{\text{dnc}} = \frac{4.0 \text{ pF}}{2.7 \text{ pF}} \text{ var.}$

$$\frac{\Delta f}{\Delta C_{\text{dnc}}} = \frac{1}{C_F^2 \cdot W \cdot L \cdot 2\pi} = \frac{90 \text{ MHz}}{\text{pF}}$$

to nearest  $4.8 \text{ MHz} \Rightarrow \Delta C_{\text{dnc}} = 5.3 \text{ pF}$ .

the range.

$$\begin{aligned} C_F = +10\% & \Rightarrow C_F = 3.63 \text{ pF} \Rightarrow C_{\text{dnc}} = 2.77 \text{ pF} \cdot 3.2 \text{ pF} \\ L_F = +10\% & \Rightarrow C_F = 3.00 \text{ pF} \Rightarrow C_{\text{dnc}} = 4.77 \text{ pF} \cdot 4.9 \text{ pF} \\ C = -10\% & \Rightarrow C_F = 2.97 \text{ pF} \Rightarrow C_{\text{dnc}} = 4.77 \text{ pF} \cdot 4.9 \text{ pF} \\ L = -10\% & \Rightarrow C_F = 2.97 \text{ pF} \Rightarrow C_{\text{dnc}} = 4.77 \text{ pF} \cdot 4.9 \text{ pF} \end{aligned}$$

$C_{\text{dnc}}$  has same  $+10\%$ .

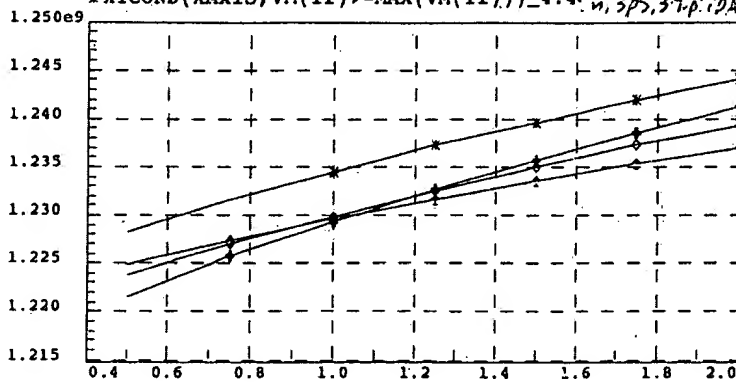
$\Rightarrow 2.7 \text{ pF} \rightarrow 2.97 \text{ pF}$  in  $5.3 \text{ pF}$  spec.

$\Rightarrow \Delta C = 2.7 \text{ pF} + (0.263) \times 4.9 \text{ pF}$

$\Rightarrow \Delta C = 2.7 \text{ pF} + (0.763) \times 4.9 \text{ pF}$

Res Hs with previous values. (Side Vector: 1/5 side).

$\circ$  XYCOND(XAXIS, VM(T1))>=MAX(VM(T1))\_1:4Sn, 3p3, 4p0  
 $\diamond$  XYCOND(XAXIS, VM(T1))>=MAX(VM(T1))\_2:4Sn, 3p6, 3p2  
 $\pm$  XYCOND(XAXIS, VM(T1))>=MAX(VM(T1))\_3:4Sn, 3p0, 4p8  
 $\times$  XYCOND(XAXIS, VM(T1))>=MAX(VM(T1))\_4:4Sn, 3p5, 3p7, 2p2

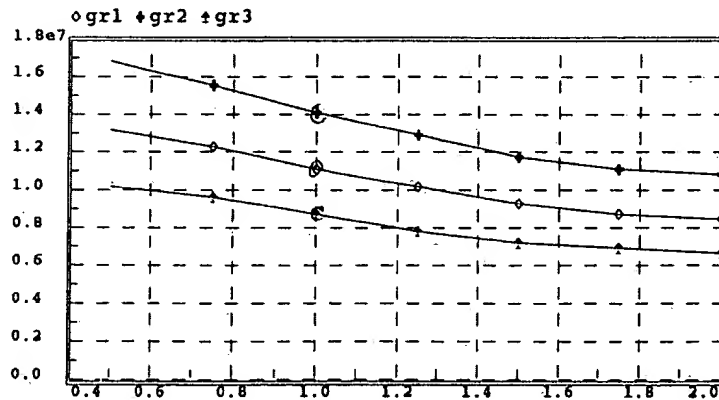


$\rightarrow$  trace = check of MHz/pF

$\approx 5 \text{ MHz/pF}$

$\approx 100 \text{ MHz/pF}$

(calculate: 90)



$9-714 \text{ MHz/V}$

Assume  $L = 120 \text{ E}$ .

$\Rightarrow$  Lt from 5.6 to 8.1 pF.

$\Rightarrow$  Cdie from 2.6 to 5.6 pF.  $\pm 10\%$   $\Rightarrow$  nominal from 2.4 to 6.2 pF.

in 65 steps  $\Rightarrow$  min 60 pF/step

$\Rightarrow$  max of 65 pF/step

$\Rightarrow$   $\Delta$ ke of  $\frac{6 \text{ MHz}}{9 \text{ MHz/V}}$

$= 0.67 \text{ V}$

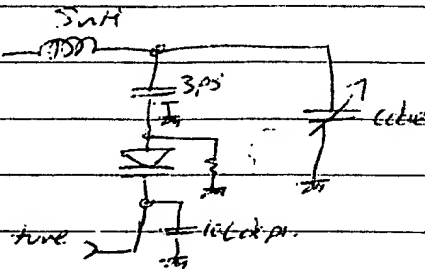
$\Rightarrow 0.3 \rightarrow 1.5 \text{ V}$

Simulations suggest 2.2 pF +  $(0.6763) \times 70 \text{ pF}$ .

high  $\Rightarrow$  2.4 pF required from  $\Rightarrow$  2.2 nV.

\*  
Trim network for VCO.

Variable  $C_v \approx 25 \text{ pF}$  series with  $3.3 \text{ pF}$  caps in parallel with CDAC,  
6-bit range  $2.2 \rightarrow 6.6 \text{ pF}$ ,  $90 \text{ fF/LSB}$  max.  $\times 2$  off, one on  
each side of Pierce circuit.



Cv out:  $Q > 20$  at  $1.2256 \text{ MHz}$ .

assume resistance dominated by  $\text{fet}$ ,  $70 \text{ fF max} \Rightarrow 77 \text{ fF max}$ .

$R_{SW} < 80 \Omega$ .

$$\Rightarrow \frac{W}{L} > 40 \text{ say } 50 \Rightarrow 18 \text{ } \cdot 35.$$

$$C_{eff} \approx 10 \rightarrow 20 \text{ fF}$$

$$\Rightarrow \text{unit} = \frac{90}{100} \text{ fF to give } D \text{ of } 90 \text{ fF.}$$

Band from  $180 \text{ fF unit} + 2.2 \text{ to } 6.6 \text{ LSB}$



Test Chip - BiCMOS.

Wk 16  $\rightarrow$  tape out (3 1/2 wks away).

Wk 18  $\rightarrow$  process start.

Charge Pump:- 250 pA full switch.

30 March 99.

VDD resize.

Assume inductance of 4.9 nH has F20% tolerance and Q of 5  $\pm$  20%  $\Rightarrow$  Model as variable L, fixed R.

Core has Q  $\gg$  15.

typical case:  $\text{previse } g_m > 10.5 \text{ mA/V}$  for  $g_{m1} \gg 1$ .  
(excluding Q of CMAC)

low  $g_m$  case  $\text{previse } g_m > 17 \text{ mA/V}$   
(including Q of CMAC)

worst case.  $\text{previse } g_m > 7.3 \text{ mA/V}$ .  
(excluding Q of CMAC)

Device device sizes, require  $g_{m1} (g_m) \gg 1.5$  for osc.

aim for  $g_m \gg 2$ .

$\Rightarrow$  each device to have  $g_m$  quoted above.

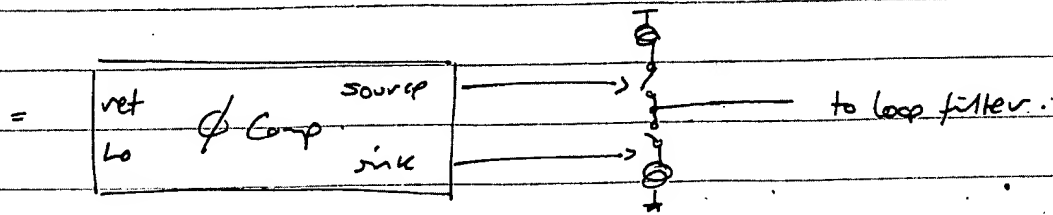
Assuming  $k'$  from 100  $\rightarrow$  200  $\mu\text{A/V}$

AV of 0.4V max  $g_m$  17 mA/V

$\Rightarrow \frac{220}{35} \text{ nA at } \approx 5 \text{ mA}$ .

Simis  $\Rightarrow$  OK.

See ~ testchip/analysis/schematic/analysis/



Phase comparator, test digits, essentially two D-type comparators turned from ~~two~~ NAND gates. Reset signal applied directly to outputs as opposed to standard scheme where only 'ripples' through D-types. Reset pulse causes both outputs to become active - extended to allow current sources to switch cleanly hence reduce deadband (0 phase offset) problems.

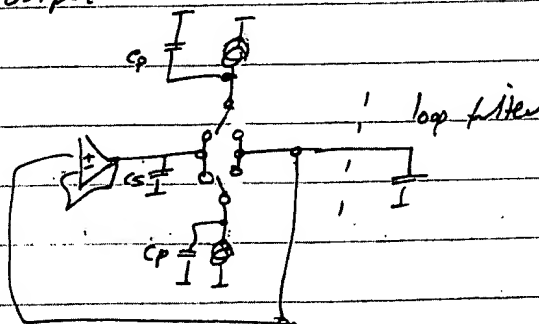
i.e. structure developed on 'Page-in-a-book' project.

### Charge pump output:

to minimise current due to charging/discharging parasitic capacitances of current sources, and reduce turn-on/off times of current sources, leave current sources on and minimise voltage change across them during switch.

### Two standard approaches.

i, Buffer output voltage and switch currents to this also not switched to output.

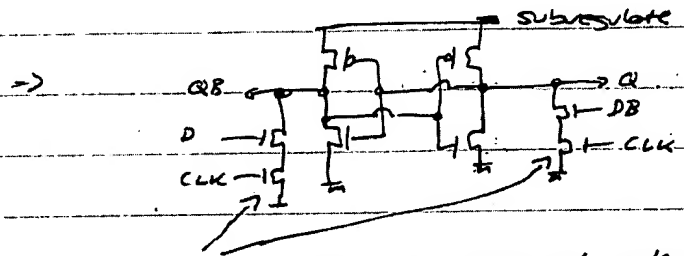


When a current source is switched to the output the voltage across the current sources is largely unchanged.  $C_p V$  small  $\Rightarrow I_{switch}$  small. Also turn off-turn-on-turn-off-turn sequence on switches to give similarly small switching current due to charge injection (lagged degree of cancellation).

Prescaler.Fast divider:- fixed scheme.

idea. formwork latch from two cross coupled inverters. Set the current in there by subregulating their supply voltage.

for driver bias such that at quiescent it can sink as much current as the p-device sources.



= 64/65.

as previously used follow a dual modulus 4/5 with a divide by 16 and decode logic such that 4/5 may only divide by 5 as we are stuck at the 16.

-ve edge faster  $\Rightarrow$  use -ve edge as trigger between blocks and at output.

What maximum set-up time for modulus control  $\Rightarrow$  last slot of 16 before output changes, also required to have 4/5 decode it doing a 4 or 5 divide on its state immediately before its output changes. ( $\therefore$  5 with odd pulse after output has changed.)

20 April 99.

Information required from S.T.

1, Layout related for test chip on bicmos.

a, Details of protection structures + requirements for pad cells which are drive devices which are within a pad.

is an example analogue output pad / input pad available in both schematic (+COL) + layout form.

b, Details of supply protection scheme; + cells (layout, COL + schematic) for use on test chip.

c, Digital cells - ST to place, or

or - us to place but require layout and cell. of cells.

- library details.

2, General.

a, Process details.

require Inductors; Poly-poly capacitors; RHPolys resistors and standard devices from HCMOS6. Please confirm.

b, Documentation. We have: - Bicmos design rule manual, 0073470 rev C.

HCMOS6 design rule manual, 00909468, rev C.

Model kit, COR96-043, rev E.

Are these up to date?

Have seen (Tat-plate) STRM6000 rev 2.0.

library reference manual. - circuits + specs.

- functions + specs.

0-35um libraries user manual, rev 1.0

c, NEXT - in COL format.

ii, layout devices to be included? Notes which protect gate - capture notes.

ELab → Cedit schematic conversion.

7 May 99.

currently all components are intrinsic calls to subcircuits which map on to primitives, elab does the mapping.

For C-Edit, need to either derive a mapping - can it handle passing parameters? or convert the netlist.

Convert netlist is probably easiest.

Rules:

'X -' removed.

'NFIN0' → '\$ NFIN0'.

~~it would also want to replace~~ 'W=' by '\$W=' for resistors and capacitors.

↓ resistors and capacitors → + third terminal to be removed.

Tuesday Meeting -

10 May 99.

NDA - sort circuit with Paul Egan

Sort out pads (analogue in/out) + supply protection.  
+ hole for digits - with parts.

KE - need to finish - peg as problem of amplitude problem.

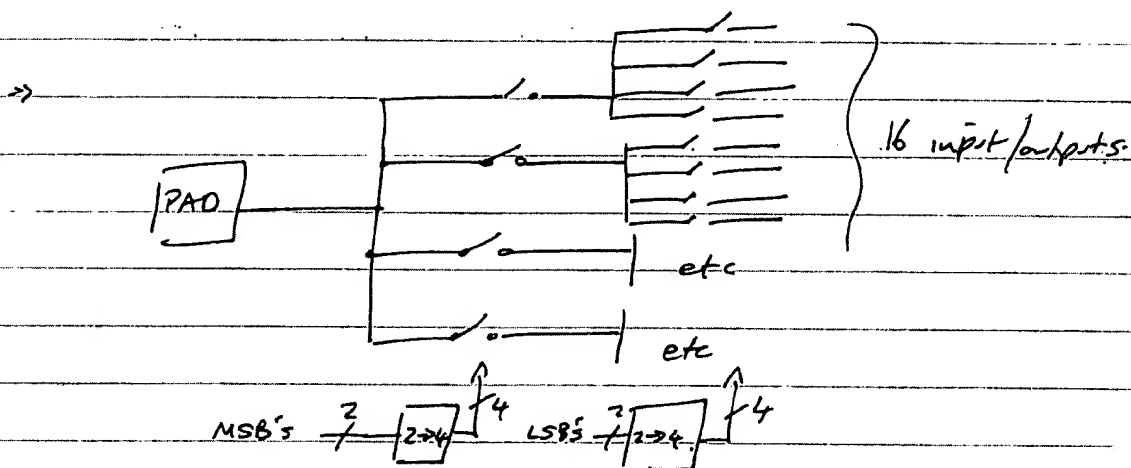
## Analogue multiplexer pad, AMUX-PAD.

20 May 99:

Orig layout found design was too large to fit in a standard pad outline and require a wider pad width. Rtg. very tight.

Design based upon  $4 \rightarrow 16$  decoder and 16 analogue switches.

For future build with two  $2 \rightarrow 4$  decoders and two sets of analogue switches in series:  $\Rightarrow$  less gates, + less routing signals (control signals).



$\Rightarrow$  factor of 2 increase in switch resistance (for same 570 degrees in analogue switches)

Testchip on ST BiCMOS process  
virtually complete.

17 June 1994.

Points worth noting:-

BiCMOS layers used:-

NWELL ONLY in VARACTOR DIODES.  
(explicit). BURIED-N+ in VARACTOR DIODES.  
SINKER in RF PADS and VARACTOR DIODES.

HMOS 6 cells. (modified).

VSS protection diodes.  
VDD protection (MOSFET protection) cell.  
~~Analogue pads~~

} All ~~parts~~ modified in Metal layers.

Modified BiCMOS 6 cells.

Analogue pads PP diodes have had Buried N, Sinkers and  
Nwell only layers removed.

NOTE: these diodes are larger area than the HMOS6  
equivalent.



## Two tone distortion products (again)

15/11/99

Two tone input, two tones at different frequencies and amplitudes.

$$\text{Input} = A \cos \omega_1 t + B \cos \omega_2 t, \text{ response } x + \kappa x^3$$

remember

$$\begin{aligned}\cos(A+B) &= \cos A \cos B - \sin A \sin B \\ \cos(A-B) &= \cos A \cos B + \sin A \sin B\end{aligned}$$

$$\Rightarrow \text{Output} = (A \cos \omega_1 t + B \cos \omega_2 t) + (A \cos \omega_1 t + B \cos \omega_2 t)^3$$

expand  $\Rightarrow$

$$\cos \omega_1 t \left[ A + \kappa A^3 \frac{3}{4} + \kappa \frac{3}{2} B^2 A \right] + \cos 2\omega_1 t \left[ B + \frac{3B^3}{4} + \frac{3}{2} \kappa A^2 B \right]$$

$$+ \cos 3\omega_1 t \left[ \frac{3A^3 \kappa}{4} \right] + \cos 3\omega_2 t \left[ \frac{3B^3 \kappa}{4} \right]$$

$$+ \frac{3}{4} \kappa A^2 B \left[ \cos(2\omega_1 - \omega_2)t + \cos(2\omega_1 + \omega_2)t \right]$$

$$+ \frac{3}{4} \kappa B^2 A \left[ \cos(2\omega_2 - \omega_1)t + \cos(2\omega_2 + \omega_1)t \right]$$

Our system:- At first filter have: centre = 1.5 MHz.

$\omega_1$  = 1<sup>st</sup> adjacent at 2.5 MHz

$\omega_2$  = 2<sup>nd</sup> adjacent at 3.5 MHz.

$\Rightarrow 2\omega_1 - \omega_2$  case important.

The filter structure is correct driver, distortion is dependent upon the signal levels throughout the circuit.  $\Rightarrow$  a less linear <sup>gm</sup> structure in a structure which has reduced signal levels will have similar overall performance to a structure with good linearity and large signals throughout. Filtering of off channel interferences increases throughput the filter  $\Rightarrow$  less amplitude due to attenuation hence lower signal levels.

Distortion Continued:-

21 July 99.

Review of 'filt1-gm1.in' modelling program. This is distortion at output due to non-linear gm1 for the basic filter structure, the one with similar input and output levels.

Inputs:- one channel  $-85\text{dBm} \Rightarrow 2\text{mV pk}$ .

Passive filter, 1st order cut  $2.5\text{MHz}$ .

$-39\text{dBm}$  } 1st tone  $4.5\text{MHz}$   $0.36\text{V pk} \Rightarrow 1.73\text{mV pk}$  after passive  
tones } 2nd tone  $7.5\text{MHz}$   $0.36\text{V pk} \Rightarrow 0.12\text{mV pk}$  after passive.

generates  $116\mu\text{V pk}$  at filter out for  $\kappa = 0.5$  in gm1.

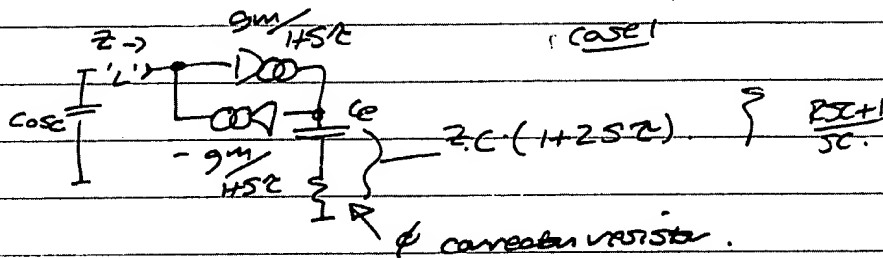
$\Rightarrow$  If this is the worst case, and transconductance elements always have  $\kappa < 0.5$  can use a basic filter structure - better for noise - and achieve linearity spec.

↓  
Noise improvement  $< 1\text{dB}$ .  $\Rightarrow$  go with more linear filter.

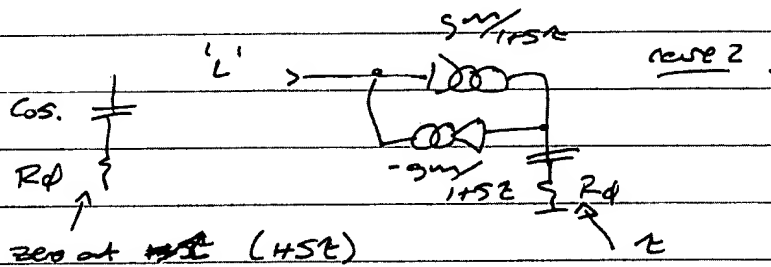
## Filters: Passive phase compensation.

26 July 99.

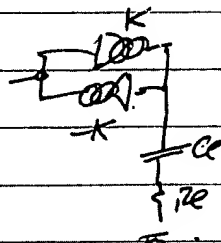
'Pass' filters were single ended. Pole caused by current mirror in transconductor altered transfer function, could be tuned out in filter component value choice but then the filter response varied unacceptably over process. Solution was to add a zero to the emulator capacitor, i.e. phase correct the inductor emulator section.



Alternative is to compensate for  $\phi$  of one  $g_m$  only and multiply response by  $(1+s\tau_c)$ .



Analysis of above :-



Case 1  $C_e R_e = 2\tau_c$   
 $\Rightarrow \frac{s.C_e}{g_m^2} + \frac{s^2 \tau_c^2 C_e}{g_m^2 (1+s\tau_c \tau_g)}$

$\frac{V_i}{i_i} = \frac{s.C_e}{K^2 (1+s\tau_c R_e)}$

$K = \frac{g_m}{1+s\tau_g}$

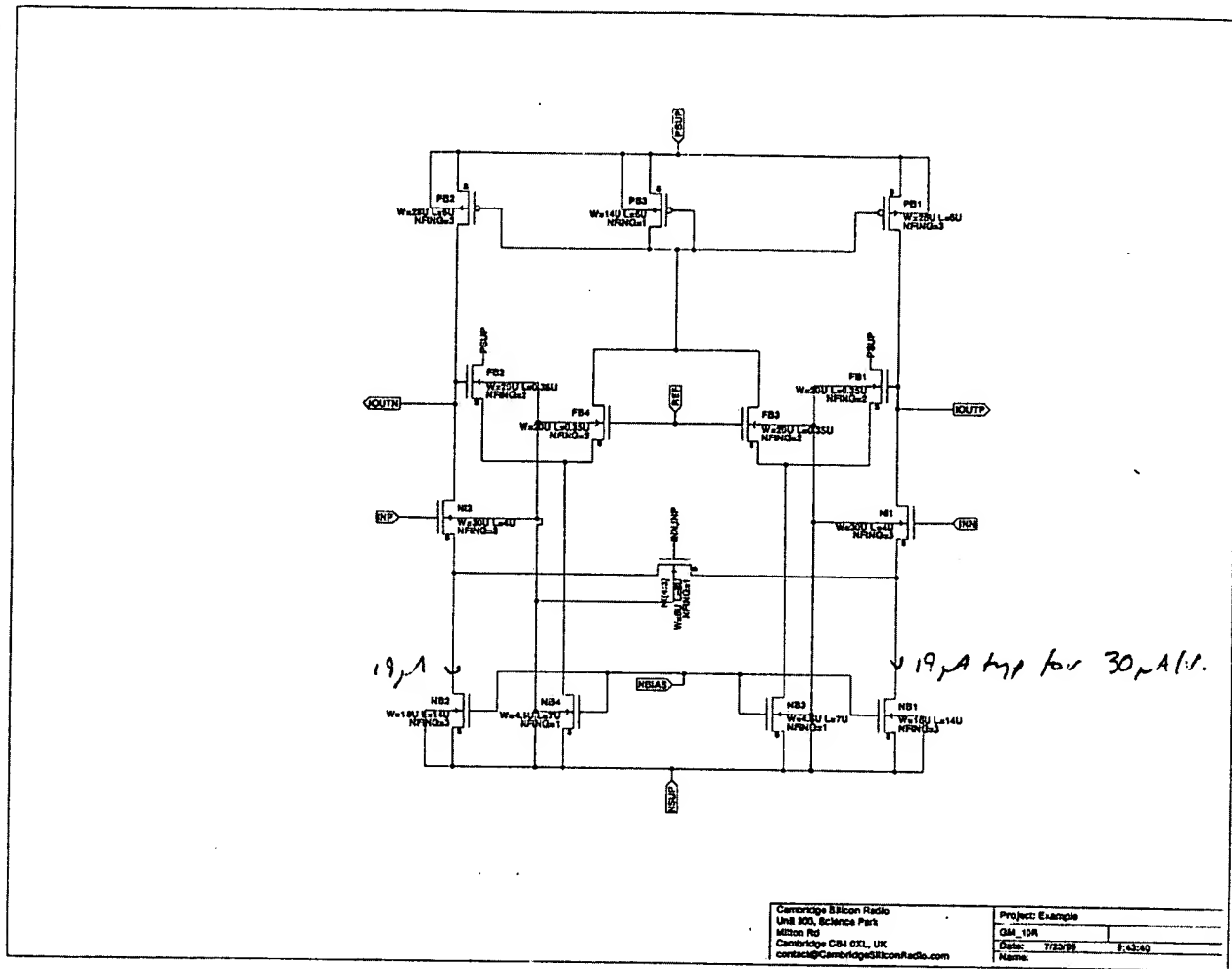
$\Rightarrow \frac{V_i}{i_i} = \frac{s C_e (1+s\tau_g)^2}{g_m^2 (1+s\tau_c R_e)}$

Case 2  $C_e R_e = \tau_g$   
 $\approx \frac{s C_e (1+s\tau_g)}{g_m^2}$

## Filter Transconductance Amplifier

28/2/99

Differential in, differential out with set point for output level.



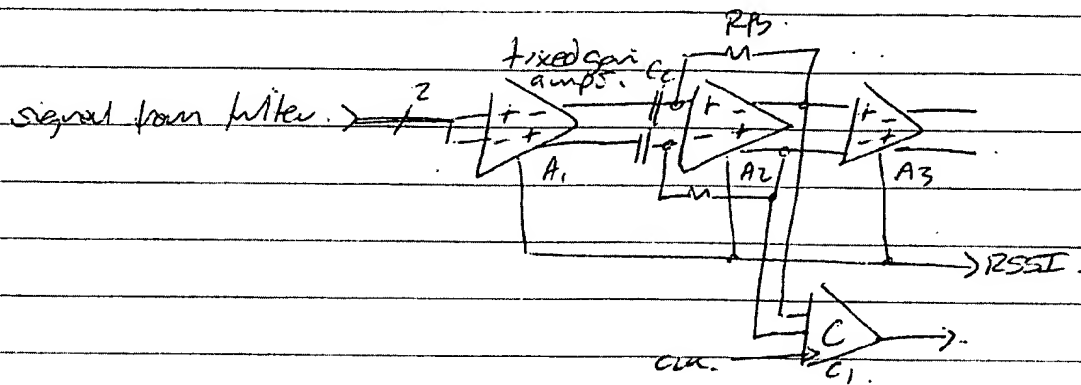
Require 28 gsm matching, right gsm for acceptable filter response. Where multiple transconductors placed in parallel get  $\times 28$  transconductance with  $\sqrt{2} \times$  variation. Hence set  $g_{m1} < 28$  for typical processing on one transconductor, should have some margin for typical process filter. Target is  $g_{m1} < 28$  over all process.

Expect better matching possible from  $C_p$  elements, so aim for 28 but accept best possible and correct in  $C_p$  elements.

Circuit above has been designed for low noise and high linearity, therefore most of its devices have large ( $4.5 - V_T$ ) values, this is good for matching  $\Rightarrow$  check  $g_{m1}$  for above and correct if necessary.

# Detector Circuitry (Timing Diagram)

12 Aug 99



fixed low gain limiting amps have limit output which generates a current when a signal input threshold is crossed,  $\Rightarrow$  output current is  $I_{out}$  and is slope, i.e.  $I_{out}$  pseudo log.

Want fast comparators, for low effective input offset and low current  $\Rightarrow$  small devices in comparators (good Bn for low current) preceded by gain (reduce input offset).

AC gain arrangement above  $\Rightarrow$  offsets of  $C_1$  and  $A_2$  and bit are divided by gain ( $A_1 \times A_2$ ). Hence for input offset of  $< 0.4 \text{ mV}$  and gain per stage at 6, offset error as high as  $14.4 \text{ mV}$ !

Required output is 4 bit word, provides four samples of a 4 phase clock. MSB to be <sup>most recent</sup> first sample. Data Rate 16 MHz. (4 bits).

$\Rightarrow$  either one comparator at 64 MHz or 4 comparators at 16 MHz.

Current consumption not linear with frequency (especially with logic for generating fast stable signals)  $\Rightarrow$  choose 4 comparators option.

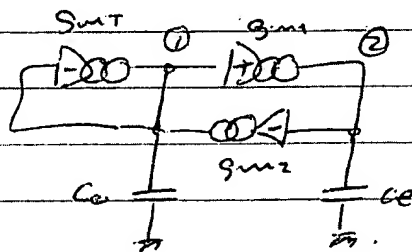
All pass filter (update).

31 Aug 99.

require transfer function of form

$$\frac{s^2 + bs + c}{s^2 + bs + c}$$

Consider:-



$$Y = \begin{matrix} & 1 & 2 \\ \begin{matrix} 1 \\ 2 \end{matrix} & \begin{vmatrix} g_{m1} + sC_1 & g_{m2} \\ -g_{m1} & sC_2 \end{vmatrix} \end{matrix}$$

$$Z_{11} = \frac{sC_1}{s^2C_1C_2 + sC_1g_{m1} + g_{m1}g_{m2}}$$

$$s^2C_1C_2 + sC_1g_{m1} + g_{m1}g_{m2}$$

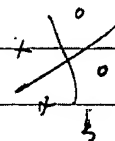
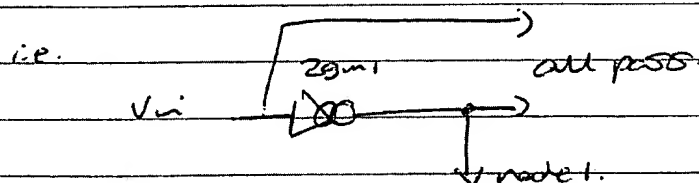
$$\therefore 1 - 2g_{m1}Z_{11} = \frac{s^2C_1C_2 - g_{m1}sC_1 + g_{m1}g_{m2}}{s^2C_1C_2 + g_{m1}sC_1 + g_{m1}g_{m2}}$$

= all pass.

→ divide node 1 with

a current and monitor voltage difference between

input voltage  $\frac{V_{in}}{2g_{m1}}$  and  $V_1$ .

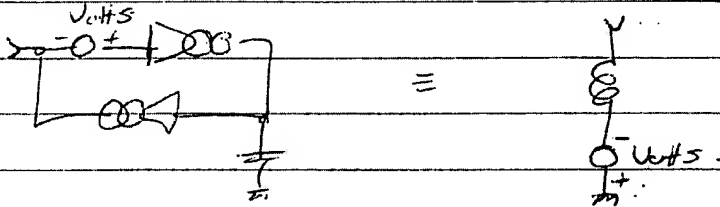


DC correction circuit:-

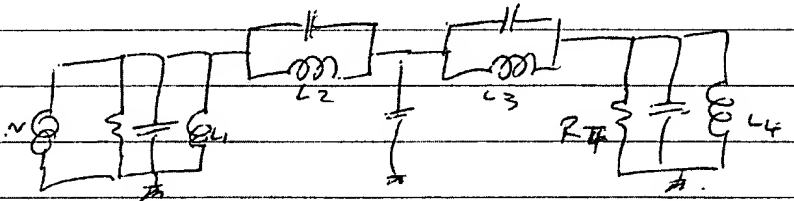
7 Sept.

The 2.5 MHz bandpass filter contains four inductors in a ring.

The gyr-C inductor realization of an inductor contains an offset voltage due to offset voltages in the transconductors which form it:-



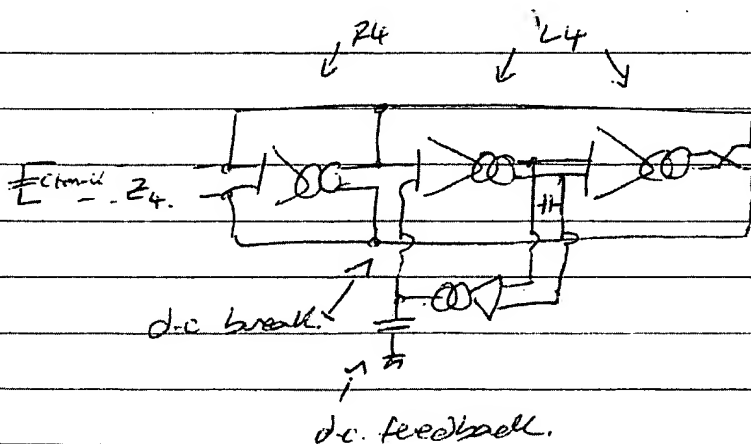
Filter Structure:-



$\Rightarrow$  Need dc break in  $L_1, L_2, L_3, L_4$  loop.

Put d.c. break in  $L_4$ :-

$L_4 + R_4$  with d.c. break.



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